B1

6, 2000; and "Software Management Tree Implementation for a Network Processor", serial number 09/545,1000, filed April 6, 2000. Each co-pending patent application is hereby incorporated by reference into this description as fully as if here represented in full. --

Page 2, amend the paragraph beginning at line 1 as follows:

B2

– The demand for hardware-integrated processing to support more and more complex tasks at media speed has led to the creation of network processors. Network processors provide wirespeed frame processing and forwarding capability with function flexibility through a set of embedded, programmable protocol processors and complementary system coprocessors. Network processors are expected to become the fundamental network building block for network devices in the manner that microprocessors are for today's personal computers. Network processors offer real-time processing of multiple data streams, providing enhanced security and IP packet handling and forwarding capabilities. In addition, they provide speed improvements through advanced architectures, such as parallel distributed processing and pipeline processing designs. These capabilities can enable efficient search engines, increased data handling throughput, and provide rapid execution of complex tasks. The programmable features of network processors provide network product developers an easier migration path to implement new protocols and technologies without requiring new custom Application Specific Integrated Circuit (ASIC) designs. --

Page 4, amend the paragraph beginning at line 4 as follows:

B3

– A typical system developed with a network processor uses a distributed software model, with each programmable network processor executing tasks concurrently. Some functions are performed in the control point (CP) processor, which can be internal or external to the network processor. The CP processor provides support for layer 2 and

B3 layer 3 routing protocols, and layer 4 and layer 5 network applications and systems management. Wirespeed forwarding and filtering functions are performed by a combination of the network processor hardware and resident picocode.

Page 21, amend the paragraph beginning at line 20 as follows:

B4 – The network processor 10 usually resides on a subsystem board and provides the protocol layer(i.e., layer 2, layer 3, layer 4 and higher) frame processing. Software running on a CP processor 34 in the CP subsystem provides the management and route discovery functions. The CP code, picocode running on the protocol processors, and picocode running on the guided frame handler enable initialization of this system, maintenance of the forwarding paths, and management of the system. As a distributed system, the CP processor and each network processor subsystem contain multiple processors which operate in parallel and communicate using guided frames for increased efficiency and performance. –

Page 29, amend paragraph beginning at line 6 as follows:

B5 -- For LPM trees, the input key will be hashed into a HashedKey 106, as shown in Fig. 5. In the preferred embodiment, no hash function is performed on the input key for LPM trees, and the hashed output equals the input key. The hash algorithm (including no hash for LPM trees) that will be used is specified in the LUDefTable. –

Page 30, amend paragraph beginning at line 7 as follows:

B6 – If colors are enabled for the tree, which is the case in the example of Fig. 5, the 16-bit color register 124 is inserted in the 176-bit hash function output and the file result is a 192-bit number, called the HashedKey 106. The insertion occurs directly after the direct table 108. If the direct table 108 contains 2^N entries, then the 16-bit color value is